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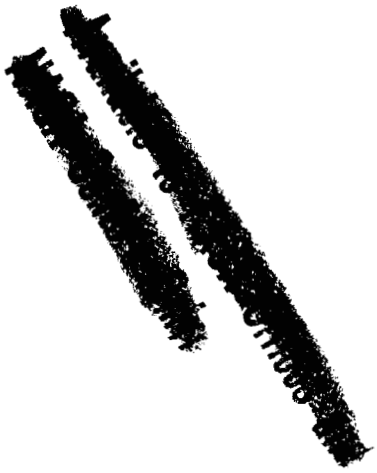
RESEARCH ON FAILURE FREE SYSTEMS

Quarterly Report No. 5

Covering the period October 20, 1964 to January 20, 1965

Prepared for:

The National Aeronautics and Space Administration
Washington, D. C.



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Report Objective and Contract Status Statement

This quarterly report is prepared in accordance with the requirements of contract NASw-572, "Research on Failure-Free Systems", between the Westinghouse Electric Corporation and the National Aeronautics and Space Administration. The report describes the work which has been done on the four major tasks described by Amendment No. 1 of this contract. The period covered by this report corresponds to the third quarter of the contract extension established by the same Amendment. The work to date represents completion of approximately 70% of the anticipated effort.

A. PROGRAM OBJECTIVE

The general objective of this research program is to consider new techniques which are expected to result in significant increases in the reliability of vital electronic systems. These increases will be realized by giving the systems the capability to withstand a large percentage of internal component failures without loss of system functional operation. The scope of this program includes the study of error detecting and error correcting codes, the problems associated with the operation and maintenance of redundant equipment, new schemes for permitting redundant system reorganization in response to changing failure patterns, adaptive logic networks and others.

B. ACTIVITY BY TASKS

The four major tasks of the current contract extension are:

I. Statistical measure of quality
II. Adaptive voter
III. Failure responsive system organizations
IV. Medium communication

A brief summary of the progress made to date and the work proposed for each of these tasks is presented in the following paragraphs.

Task I. Statistical Measure of Quality

The object of this task is to develop a method for accurately evaluating the reliability of redundant systems which may contain internal component failures at the time the evaluation is made. Particular attention is to be given to making high confidence system reliability estimates based on the analysis of results obtained from testing only selected subsystems. Because of the high cost associated with exhaustive system tests, reliability estimates, based on partial system testing of this type, will soon be essential for the effective use of redundant systems.

To consider more complex systems with greater generality and flexibility, assumption one, stated in Quarterly Report No. 4, has been relaxed. This change is reflected in the description of subtask number one found below. The subtasks listed below are currently being performed:

1. The system model considered in this task has n independent stages. Each stage (i) consists of (n_i) identical units. The number of working units required for successful operation of a stage may vary from stage to stage. The model is being analyzed to derive general expression(s) for the probability of system success for any mission time t_m. The expression(s) will reflect the results of testing selected subsystems prior to any mission

phase. In addition, the expressions will provide a lower confidence level probability estimate for the case in which no tests are made just prior to the mission.

2. An algorithm for the allocation of test points is being developed which considers the dual problem of optimizing the placement of test points subject to placing constraints on available dollars or the number of test points.

3. A decision model is being developed. This decision model could be used as an aid to the design engineer for determining which design configurations best approaches the optimum allocation described above.

Task II. Adaptive Voter

This task is concerned with the development of a new implementation of the restoring (or voting) circuits required by multiple-line redundant systems. It has been shown analytically that voting circuits with certain adaptive capabilities are potentially more effective in combating the effects of failures than are the currently used majority-voting circuits. The specific object of this task is to design, construct, and test an adaptive voting circuit which will include the most recent advances in adaptive circuit components.

Work on this task was begun this quarter in accordance with the original schedule. The task effort has been roughly divided into the following subtasks.

1. Development of a computer program which can:
   a. Generate multichannel simulated voter input data with selectable error rates.
   b. Perform the feedback control portion of the voter adaption process.
2. Implementation of this program on an available on-line computer.
3. Design and construction of a breadboard model of variable weight, summation, and threshold output sections of an adaptive voter.

Flow charts describing the operation of the computer program have been prepared. Arrangements have been made to secure the use of an SDS-910 computer to supply the on-line computer capability required by this task. As soon as the final details on the program are completed, the program will be coded in the SYMBOL language used by the SDS-910. This computer will be available to the engineers assigned to this task as they required it at no direct cost to this contract.

The design and construction of the breadboard model of the adaptive voter has not yet begun. Westinghouse has acquired thirty Mercury Cell Integrators for evalution in an adaptive voter circuit. The design and construction of an adaptive voting circuit which will employ these integrators is expected to take less than three weeks. The completion of this subtask is scheduled to correspond with the completion of the coding portion of the programming effort.

Task III. Failure Responsive System Organizations

This task is intended to be a continuation of the "Self-Repairing Systems" study which began during the first year of this contract. It was shown in that study that systems which have the capability to partially reorganize their redundant subsystems in response to existing internal failure patterns may be more resistant to early life system failures than comparable fixed redundant systems. The first goal of this study is to develop design rules and implementation techniques which will make such systems practicable. The second goal is to design a specific study vehicle which can be used to demonstrate the feasibility of such systems.

The majority of the effort performed on this task during this quarter has been oriented toward the design of the study vehicle. The design rules developed during the two preceding quarters have been used as a basis for the study vehicle design. The switching strategy incorporated in the design is the "step list" pattern. This is one of the better strategies developed during the simulation study. Three "spares" are provided for each stage in the system, with all spares having exactly the same mobility.

After an extensive investigation it was decided that the type of system which would best demonstrate the feasibility of the failure response techniques would be a special purpose arithmetic unit.

The specific study vehicle which has been selected is the arithmetic section of a beam-steering computer from a phased array radar. This unit receives data, performs a number of arithmetic operations on the data, temporarily stores, and then reads out the results. The arithmetic unit, which must provide a given sequence of operations properly timed in relation to inputs and outputs, plus storage of intermediate results during computation, was chosen to tax both the reorganizational strategy theories and the implementation techniques which have been developed.

The beam-steering computer consists of four identical subsystems, each consisting of two adder-subtracters, two shift registers, and one full adder. The circuitry required to implement a single subsystem consists of 33 gates and 31 flip-flops. The system operates on a three phase cycle: input data read-in, arithmetic computation and storage, and results output.

This study vehicle design is intended to demonstrate that the failure responsive techniques provide an extremely powerful tool for increasing the useful life of digital systems. The application of failure responsive techniques to this study vehicle demonstrates the capability of the technique to:

1. Detect errors in subsystem output
2. Perform necessary switching of "spares" to replace failed subsystems
3. Reorganize systems containing memory (in cases in which the memory state is input - controlled)
4. Switch subsystems which perform slightly different functions, depending on the stage in the system in which they are operating.

The detailed logic design of the study vehicle is nearing completion. The design will contain sufficient detail that a breadboard model can be constructed directly from the design specifications.

Task IV. Medium Communication for Module Reorganization

The primary goal of this task is to explore the advantages and limitations of systems whose component subsystems communicate through a medium or media other than wired and switched signal paths. The investigation will include consideration of various potential media and establishment of the general characteristics required of subsystems which communicate through a common medium.

The effort on this task has been concentrated on the exploration of systems whose component subsystems communicate through a medium of memory cells. The investigation has shown that such systems offer the following potential advantages over systems having a fixed communication channel implementation.

1. Error-detection and correction may be done by a small "pool" of voters during the time information is stored in the medium
2. The subsystems do not have to be continuously synchronized to a common timing (or sync) source
3. The effect of redundancy may be achieved with little or no redundant equipment through a time sharing technique
4. Graceful degradation is almost inherently achievable
5. The entire communication linkage pattern may be changed through a process similar to that of reprogramming a general purpose computer.

To realize the advantages offered by systems of this type, constraints must be placed on the component subsystems and upon the types of problems which the systems can handle. The subsystems are subject to the same homogeneity restrictions to which the wired failured responsive systems are subject. For most systems, this implies that a general purpose subsystem must be devised which contains a storage register and an internal function decoding network. The latter items are required to specify the exact operation of the subsystems for each of their possible locations within the system. Also in this category is the requirement that any memory within the subsystems must be controlled by the input data stream.

The problems handled by these systems must be such that the data associated with the problem can be processed in "word" units by individual subsystems. Within each subsystem, the words may be treated on a "bit" by "bit" basis, but the characteristics of most applicable types of electronic memories only facilitate the efficient data transmission in a "word" by "word" mode of operation.

An effort has been made to develop the general plan of a system using a memory as the communication link between subsystems. Although this effort is still in the early stages of development, the use of a drum memory with its mechanical scan characteristics seems to offer at least one feasible approach to the implementation of such systems.

C. MANAGEMENT AND PERSONNEL

The management of this contract continues to be performed by the Advanced Development Subdivision of the Surface Division of the Westinghouse Electric Corporation. The management and advisory personnel with primary responsibility for this program include:

Mr. Sidney E. Lomax, Director of Development
Mr. Henry F. DeFrancesco, Advisory Engineer

The technical personnel assigned to the program during this contract quarter include:

Mr. Charles G. Masters, Jr., Project Engineer
Mr. Joseph M. Hannigan
Mr. Faris T. Kahwajy
Mr. William A. Lutts
Mr. Kevin P. Shambrook
Mr. James E. Thompson
Mr. Karl C. Wehr